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PATENT NUMBER and  
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10052063	FILING DATE 01/16/2002	CLASS 710	SUBCLASS 738	GAU 2182	EXAMINER <i>[Signature]</i>
<b>**APPLICANTS:</b> Cheah Jonathon; Quek Chee; Kwek Ee; 714 9167 2133					
<b>**CONTINUING DATA VERIFIED:</b>					
<b>** FOREIGN APPLICATIONS VERIFIED:</b>					
PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input checked="" type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO 004939P025	
Verified and Acknowledged Examiners's initials					
TITLE : In-chip monitoring system to monitor input/output of functional blocks					
U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)					

<b>NOTICE OF ALLOWANCE MAILED</b>		<b>CLAIMS ALLOWED</b>	
		Total Claims	Print Claim for 0.6
<b>ISSUE FEE</b>		<b>DRAWING</b>	
Amount Due	Date Paid	Sheets Drawn	Figs. Drawn
		Print Fig.	
<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>		<b>Application Examiner</b>	
		<b>PREPARED FOR ISSUE</b>	
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